REMARKS

Claims 1-29 remain in the application. Claim 14 has been amended to correct a minor informality.

Claim Rejections under 35 U.S.C. § 112

Claims 1-29 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement and as failing to comply with the enablement requirement.

Claims 1-29 were rejected under 35 U.S.C. § 112, second paragraph as failing to distinctly claim the invention.

As described in the Background section, branch prediction is "one of the most important contributors to processor performance." (para. 0006). Branch prediction is well-known in the art. The Background section describes two predictors and their operation. A simple predictor is one that produces a prediction in a relatively quick amount of time including just one cycle (see para. 0008). As the predictor takes on more input data such as global branch history, indirect branching, and return branching, the predictor becomes more complex (and more accurate) and would take longer than one cycle to produce a prediction. (Id.). The more clock cycles that are needed to make a prediction, the more throughput or bandwidth of the processor may be affected. (Id.).

Since branch prediction is known, the specification focuses on affecting the inputs and outputs of such devices to achieve an improvement in processor performance. For example, independent claim 1 recites as follows:

1. A method of predicting instruction branches, comprising:

generating a current next-line prediction based on a previous next-line prediction; and

generating a current checking prediction based on the previous next-line prediction; and

generating a subsequent checking prediction based on the current next-line prediction, the checking predictions being independent from one another and having a longer latency than the next-line predictions.

Support for the claim includes Fig. 2, which shows a branch prediction architecture and Fig. 3, which shows a flow diagram for the generation of next-line predictions and checking predictions. The method steps are clearly supported by the specification as filed. The Office Action specifically points to a "checking predictor" and states that one is not described in the specification to enable one skilled in the art to make and use such a device. Applicants respectfully disagree. Paragraphs 0007-09 of the Background section describe systems that include next-line prediction and checking prediction and a description of what predictions are being made and what inputs are used to make such predictions. Since next-line predictors and checking predictors are known in the art, one skilled in the art with respect to branch prediction would understand how to construct such devices. An example of the prior art is U.S. 5,283,873, which describes next line prediction (element 17) along with circuitry for checking the next line prediction (element 13).

Since next-line predictions and checking predictions are known in the art, the present claims, which focus on the use of such predictions are distinct in their language are, clearly

enabled by the present application. Accordingly, reconsideration and withdrawal of the rejection of claims 1-29 under 35 U.S.C. § 112, first and second paragraphs is respectfully requested.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
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